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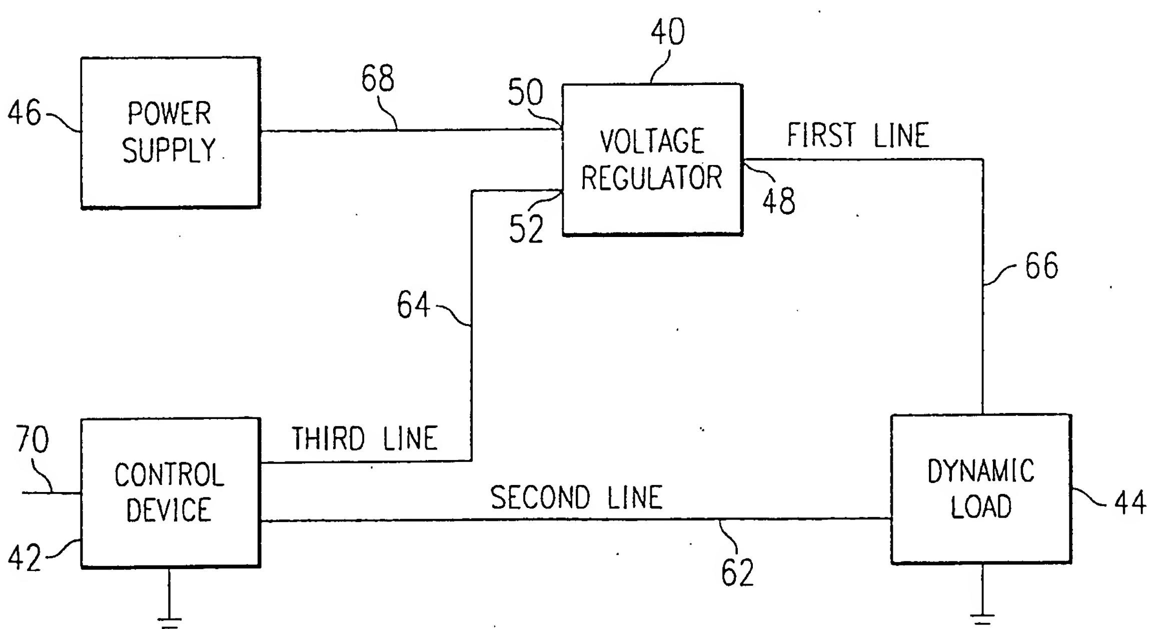
(54) Programmable bandwidth voltage regulator

(57) A method for reducing the transient response time of a voltage regulator when the load attached to it is entering or exiting a lower power consumption level by changing the bandwidth of the voltage regulator without compromising its stability, and a bandwidth regulator for implementing such a method are disclosed, wherein the bandwidth of the voltage regulator is changed based on a signal sent by a control device when it senses that the component is about to change power consumption levels.

FIG. 1



EP 0 779 568 A2

Description

The present invention relates to the field of integrated circuits, and is more specifically directed to voltage regulators.

In order to reduce power consumption many electronic components are now capable of operating at several power consumption levels, one of which is typically a power-down or sleep mode. The power-down mode is a low power consumption level that the component can enter into when it is not performing an operation or being accessed. Reducing the level of power consumption is particularly useful for battery operated devices, such as portable computers, where reducing power consumption increases the battery life, and therefore the time the device can be used without having to either replace or recharge the battery.

A microprocessor consumes a significant amount of power in the full power-up mode, and it is typically accessed only a small portion of the time, therefore it is advantageous to bring the microprocessor into the power-down mode when it is not being accessed. In the power-up mode the microprocessor can draw a current of up to 10 A. In the power-down mode the microprocessor can maintain its state with a current of as little as 100 µA (i.e. as much as 100,000 less than in the power-up mode). A power supply, such as a battery, typically supplies the current to the microprocessor through a voltage regulator. The time in which the voltage regulator can go from delivering the proper voltage for the current required in the power-down mode to delivering the proper voltage for the current required in the power-up mode, and vis versa, is the transient response time of the voltage regulator. The large change in current demand of the microprocessor, which is the load of the voltage regulator, may bring the voltage regulator out of regulation during the transient response.

The stability of the voltage regulator is primarily dependent on the size of its compensation capacitor, its load capacitor, and its pass element. The compensation capacitor is the capacitor put in at the gain stage of the voltage regulator to compensate the phase shift of the voltage regulator, and hence prevent oscillation. A larger compensation capacitor increases the stability of the voltage regulator. The size of this capacitor is inversely proportional to the bandwidth of the voltage regulator, and directly proportional to the transient response time of the voltage regulator. The larger the compensation capacitor the more stable the voltage regulator, and, unfortunately, the smaller the bandwidth of the voltage regulator. The smaller bandwidth does not allow the voltage regulator to respond quickly to large changes in current demand, increasing the transient response time.

Additionally, since the stability of the voltage regulator is dependent on the load capacitor as well as the compensation capacitor, as the load capacitor is reduced the voltage regulator becomes less stable. A smaller load capacitor is both easier to use and easier to recycle after the circuit is no longer needed, however it reduces the stability of the voltage regulator. The decrease in the load capacitor can be compensated by an increase in the compensation capacitor to ensure the stability of the circuit. However, as discussed above, an increase in the compensation capacitor reduces the bandwidth of the voltage regulator, and therefore increases its transient response time.

In some configurations proposed circuits have changed the bandwidth of the voltage regulator when the feedback loop of the voltage regulator indicated that the voltage regulator is out of regulation because of the large change in current demand. Alternative proposals have suggested monitoring circuits that could monitor the current demand of the load and notify the voltage regulator after there is a change in the current demand of the load.

A problem with the above methods is that during the time that the change in current demand is going through the feedback loop, or by the time the monitoring circuit detects that the current demand of the load has changed, the load is not receiving the appropriate voltage. The present inventor has observed that another problem is that during the time it takes to detect the change in the current demand the load is not receiving the proper voltage due to the large current demand, the voltage regulator does not know that it is not delivering the required voltage and has not even changed its bandwidth, thus increasing the transient response time by this amount of time.

Further background on voltage regulators and on stability criteria of analog devices can be found in Grebene, Alan B., BIPOLAR AND MOS ANALOG INTEGRATED CIRCUIT DESIGN, John Wiley & Sons, 1984; Gray, Paul R. and Robert G. Meyer, ANALYSIS AND DESIGN OF ANALOG INTEGRATES CIRCUITS, 2nd ed., John Wiley & Sons, 1984; Franklin, Gene F, et al., FEEDBACK CONTROL OF DYNAMIC SYSTEMS, Addison-Wesley Publishing Co., 1986; SGS-THOMSON, Microelectronics, Inc. databooks for voltage regulators, for linear ICs, and for automotive products: and National Semiconductor databooks, datasheets and application notes for voltage regulators, all incorporated herein by this reference.

The present application discloses methods and circuits for reducing the transient response time of a voltage regulator when the load attached to it is entering or exiting a lower power consumption level, without compromising the stability of the voltage regulator. A control device is connected to both a voltage regulator and a dynamic load. When the control device senses that the dynamic load should change its power consumption level it sends a signal to a regulation means in the voltage regulator to change the bandwidth of the voltage regulator to be able to deliver the required voltage in the shortest possible time. At the same time (or shortly thereafter, depending on the requirements of the system) the control device sends a signal to the dynamic

load to change its power consumption level. In one sample embodiment of the invention, after the voltage regulator starts delivering the required voltage the regulating means returns the bandwidth of the voltage regulator to the optimal bandwidth for the dynamic load connected to the voltage regulator.

In one embodiment of the invention the regulating means includes a way of switching the compensation capacitor in or out when the control device signals the voltage regulator to change the bandwidth of the voltage regulator. In another sample embodiment of the invention the regulating means includes a switched capacitor that changes the bandwidth of the voltage regulator when the current demand of the load is about to change.

One advantage of the present invention is that the bandwidth of a voltage regulator can be increased in order to reduce the voltage regulator's transient response, without compromising the voltage regulator's stability.

Another advantage of this invention is that there is no delay time from the time the current requirement of the dynamic load increases until the time the bandwidth of the voltage regulator increases, to allow the voltage regulator to deliver the required voltage faster.

A further advantage of this invention is that it allows a load to enter the power-down mode faster, reducing the power consumed by the load.

Another advantage of this invention is that it allows the use of a smaller load capacitor without compromising the stability of the voltage regulator.

A particularly advantageous use of the current invention is in battery-powered, portable computers. The improved transient response time of the voltage regulator allows aggressive power-conservation strategies in which the microprocessor frequently enters sleep mode.

Other advantages and objects of the invention will be apparent to those of ordinary skill in the art having reference to the following specification together with the drawings.

Some embodiments of the invention will now be described by way of example and with reference to the accompanying drawings in which:

Figure 1 is a block diagram of a electrical system of the present invention.

Figure 2 is a block diagram of a computer.

Figure 3 is a timing diagram of the electrical system of the present invention.

Figures 4a, 4b, and 4c are schematic diagrams of a voltage regulator formed according to embodiments of the present invention.

Figure 5 is a schematic diagram of a voltage regulator formed according to another embodiment of the present invention.

Figure 6 is a schematic diagram of a voltage regulator formed according to another embodiment of the present invention.

Referring to Figure 1 an electronic system, such as a computer shown in Figure 2, which uses a power supply including a voltage regulator according to the preferred embodiment of the invention will now be described. A power source 46, such as a battery, supplies a constant, unregulated voltage to the voltage regulator 40 through the first input 50 of the voltage regulator. A first line 66 connects the output 48 of the voltage regulator 40 to the first input of a dynamic load 44.

The dynamic load 44 can be any component of the computer that can operate at either of at least two power consumption levels, one of which is preferably a sleep or power-down mode. A microprocessor can be used as a typical dynamic load 44. Many microprocessors now manufactured can operate at both a power-up mode and a power-down mode. Additionally, because microprocessors consume a significant amount of power it is advantageous to bring the microprocessor into a power-down mode when it is not being accessed. The dynamic load 44 (hereinafter referred to as microprocessor 44), has a second input connected via the second line 62 to the first output of a control device 42. A third line 64 connects a second output of the control device 42 to the second input 52 of the voltage regulator 40.

The control device 42 has a sensing means that detects whether the microprocessor 44 needs to be accessed, for example when there is an input on one of the input device, such as a keystroke, or when the microprocessor needs to access a drive. The sensing means is typically an integrated circuit dedicated to monitoring access to the microprocessor, e.g. such as a keyboard monitoring circuit or an application specific integrated circuit dedicated to monitoring access to the microprocessor, both of which are well known in the art.

Figure 3 shows the logic states of the input line 70 to the control device 42 and first 66, second 62, and third 64 lines that connect some of the elements of the electronic system. Referring to Figure 2 and Figure 3 simultaneously, one sample operation of the system will now be described. At time t_1 the microprocessor 44 is in the power-down mode and one of the components of the computer signals that the microprocessor 44 needs to be accessed. At t_2 the sensing means senses that the microprocessor needs to be accessed, typically by a change in the logic state of the input line 70, the third line 64 goes from the first logic state at which it is normally kept, preferably low, to a second logic state, preferably high. This signals the regulating means, connected to the second input 52 of the voltage regulator 40, to change the bandwidth of the voltage regulator 40 from a first bandwidth to a second bandwidth. In the preferred embodiment of the invention, when the dominant pole of the voltage regulator is produced by the compensation capacitor, the second bandwidth is higher than the first bandwidth, although under other circumstances it may be advantageous for the first bandwidth to be higher than the second bandwidth.

The first and second bandwidths are dependent on the desired operation of the voltage regulator 40 and of the microprocessor 44. In the power-down mode the microprocessor 44 draws very little current, in the present

technology the microprocessor typically draws 100 μA in the power-down mode. When the microprocessor 44 wakes up, i.e. exits the power-down mode and powers up, it starts to draw much more current, in modern technology a typical microprocessor may require as much as 10 A. The time period within which the voltage regulator needs to respond to this increase in current, i.e. the transient time, is usually short, on the order of 1 μsec with current microprocessors. The first bandwidth is chosen based on the desired stability of the voltage regulator, and typically is low. The stability of the voltage regulator 40 is dependent on the compensation capacitor, which is typically 10 pF to 100 pF, and the load capacitor, which is a combination of the capacitance of the microprocessor and any capacitors in parallel with the microprocessor 44 connected to the output of the voltage regulator 40. The capacitance of the microprocessor 44 is typically very small compared to the capacitor in parallel with it and is thus practically negligible. Therefore, the load capacitor can be fairly accurately approximated by the capacitor across the output of the voltage regulator 40, which can typically be between .1 μF to 100 μF.

A smaller load capacitor is both easier to use and is more environmentally friendly, i.e. easier to recycle after it is not needed, however it reduces the stability of the voltage regulator. The decrease in the load capacitor can be compensated by an increase in the compensation capacitor to ensure the stability of the circuit, i.e. as the load capacitor is reduced the compensation capacitor should be increased. Unfortunately increasing the compensation capacitor reduces the bandwidth of the voltage regulator, and therefore increases its transient response time. However, since the bandwidth is also dependent on the load capacitor compensation of the load capacitor is typically needed since a small load capacitor produces a higher bandwidth, which may cause instability.

The first bandwidth is chosen to insure the stability of the voltage regulator 40 based on the above relationship of the compensation capacitor and the load capacitor, and also on the capacitance of the passive element of the voltage regulator. For example, the first bandwidth can be on the order of one to several kiloHertz. The second bandwidth is chosen to allow the voltage regulator to quickly respond to the large change of current demand by the microprocessor, thus reducing the transient time. For example, for a current step of five orders of magnitude, described above, with the transient time being about 10 μsec, the second bandwidth can be in the range of 100 kHz to 1 MHz.

Referring still to Figure 2 and Figure 3 simultaneously, at t_3, the control device 42 changes the logic state of the second line 62 from the first logic state to the second logic state, signaling the microprocessor 44 to exit out of the power-down mode. This can occur at the same time as the logic state on the third line 64 changes, signaling the voltage regulator 40 to change the bandwidth, making t_3 equal to t_2, or a short period of time, for example 200 nsec, after the logic state on the third line 64 changes. Although this brings the voltage regulator 40 out of regulation, the microprocessor 44 drawing the higher current produces the same effect and the change in bandwidth allows the voltage regulator 40 to respond to the higher current demand more quickly, thus reducing the amount of time the microprocessor 44 is not getting the required voltage. In the example above the change in bandwidth is from a lower to a higher bandwidth to shorten the transient response time, although in other circumstances the bandwidth can be reduced instead of increased to produce the same effect.

When the voltage regulator 40 starts to deliver the required voltage to the microprocessor 44, at t_4, the logic state of the third line 64 goes back to the first logic state. Preferably the control means 42 changes the logic state of the third line 64 back to the first logic state after a known time interval. One skilled in the art can calculate the time interval from t_2, the time the microprocessor requires a higher current, until t_4, the time at which the voltage regulator starts to deliver the voltage required by the load, based on the bandwidth of the voltage regulator, the load capacitor, the input voltage of the voltage regulator 40, and the properties of the microprocessor 44, such as the rate at which the microprocessor's current demand changes. However, the control means 42 can change the logic state of the third line 64 based on any known means of detecting that the required voltage is being delivered, such as: monitoring the microprocessor 44 through a monitoring circuit that can sense that the microprocessor is receiving the required load, or monitoring the voltage regulator 40 through its feedback loop.

The voltage regulator 40 can now either remain at the second bandwidth or the regulating means can change its bandwidth either back to the first bandwidth, or to a third bandwidth that is optimal for the size of the load capacitor. A larger load capacitor can lower the bandwidth that allows the load to continue drawing the required current and the proper voltage without oscillating. The compensation capacitor of the voltage regulator shifts the position of the pole produced by the load capacitor to increase the stability of the voltage regulator. Therefore, if the compensation capacitor is large enough to compensate for the load, the bandwidth of the voltage regulator 40 can be returned to the first bandwidth, otherwise a second compensation capacitor that would produce a third bandwidth can be selected. The third bandwidth is based on the need for a bandwidth high enough to permit the voltage regulator 40 to deliver the required current and the proper voltage, yet keep the bandwidth as low as possible, to enhance the stability of the voltage regulator 40. Therefore, a second value for the compensation capacitor can be selected to optimize a bandwidth for the size of the load capacitor.

The transition into the power-down mode follow a similar process. The time t_5 at which the microprocessor

should enter the power-down mode is typically determined through the operating system monitoring the access to the microprocessor and determining that there has been no request to access it for a specific amount of time. At t_5 the sensing means of the control device 42 senses that the microprocessor should enter the power-down mode, typically by a change in the logic state of the input line 70 generated by the operating system. At time t_6, control device 42 changes the logic state on the third line 64 from the first logic state (preferably low) at which it is normally kept to a second logic state (preferably high). This signals the regulating means, connected to the second input 52 of the voltage regulator, to change the bandwidth of the voltage regulator 40 from the first or third bandwidth at which it is operating to the second bandwidth.

At t_7, the control device 42 changes the logic state of the second line 62 from the second logic state to the first logic state, signaling the microprocessor 44 to enter into the power-down mode. This can occur at the same time as the logic state on the third line 64 changes, signaling the voltage regulator 40 to change its bandwidth, making t_7 equal to t_6, or a short period of time. for example 200 nsec, after the logic state on the third line 64 changes. The higher bandwidth allows the voltage regulator 40 to respond to the reduction in the current demand quicker, reducing the amount of time the microprocessor 44 is getting too much current.

When the voltage regulator 40 starts to deliver the required voltage to the microprocessor 44, at t_8; the logic state of the third line 64 goes back to the first logic state. Preferably the control means 42 changes the logic state of the third line 64 back to the first logic state after a known time interval. One skilled in the art can calculate the time interval from t_6, when the microprocessor requires a lower current, to t_8, the time at which the voltage regulator 40 starts to deliver the proper voltage, based on the same criteria that the interval from t_2 to t_4 is calculated, i.e bandwidth of the voltage regulator 40, the load capacitor, and the properties of the microprocessor 44. However, this can also be done by any known means of detecting that the current and voltage required by the load are supplied. Some examples such means are: monitoring the microprocessor 44 through a monitoring circuit that can sense that the microprocessor 44 is receiving the required current and voltage, or monitoring the voltage regulator 40 through its feedback loop. The voltage regulator 40 can now either remain at the second bandwidth or the regulating means can change its bandwidth back to the first bandwidth.

Referring to Figure 4a, one embodiment of voltage regulator 40 with a regulating means for regulating the bandwidth is now described. A reference voltage generator 80 is connected between ground,. the power source 46, and the non-inverting input of the error amplifier 82. The error amplifier 82 compares the voltage generated by the voltage reference 80 and a scaled output voltage of the voltage regulator 40. The error amplifier 82 drives the gain stage 84. The gain stage 84 drives the pass element 85. Resistors 86 and 88 form a voltage divider used to scale the output voltage of the voltage regulator 40 to allow it to be fed back to the inverting input of the error amplifier 82.

The regulating means is typically in the gain stage 84 of the voltage regulator 40. In this embodiment the gain stage 84 includes an amplifier 90, a resistor 92, and a first capacitor 94, configured as a differentiator. The first capacitor 94 is the compensation capacitor. The gain stage 84 also includes a first analog switch 96. In the preferred embodiment of the invention the analog switched is connected in the manner where it minimizes the charge injection of the analog switch 96. For example in the embodiment of the regulating means shown in Figure 4a, the analog switch 96 is connected between the resistor 92 and the output of the amplifier 90.

The first capacitor 94 compensates the voltage regulator 40 increasing its stability, but decreasing its bandwidth. At t_2 and t_5, when the control device 42 signals to the regulating means to change the bandwidth of the voltage regulator when the microprocessor is about to change levels of power consumption, the analog switch 96 is opened. This changes the bandwidth of the voltage regulator 40 to the second bandwidth, thereby shortening the time in which the voltage regulator 40 can begin to deliver the required voltage, i.e., reducing the transient response time. At t_4 and t_8, when the voltage regulator 40 is delivering required voltage, the analog switch 96 is closed, returning the bandwidth of the voltage regulator 40 to the first bandwidth. Although a differentiator is used in the example above, an integrator, as shown in Figure 4b, or combination of a differentiator and integrator, as shown in Figure 4c, can be used to control the banduidth of the voltage regulator.

In an alternative embodiment a second capacitor 98 is connected in parallel with the first capacitor 94, as illustrated in Figure 5. A second analog switch 100 is connected between the first analog switch 96 and the second capacitor 98. At t_4, when the voltage regulator 40 starts delivering the proper voltage, and it is preferable to leave the voltage regulator at the third bandwidth instead of the first bandwidth to insure that is continues delivering the required voltage, the second analog switch 100 instead of the first analog switch 98 is closed.

When different dynamic loads can be attached in turn to the output of the voltage regulator 40, additional capacitors 102 and analog switches 104 can be added. Since the bandwidth of the voltage regulator 40 varies based on the size of the compensation capacitor, the capacitors can be designed to tailor the bandwidth to the optimum bandwidth for a particular load, and the capacitor associated with a particular load can be switched in when a particular dynamic load 44 is attached. At t_4, when the voltage regulator 40 starts delivering required voltage, the analog switch corresponding to the capacitor that produces the optimum bandwidth for the particular dynamic load 44 is closed.

Referring to Figure 6, in another alternative embodiment of the invention, the regulating means includes a switched capacitor 112 connected between the first capacitor 94 and the output of the amplifier 90. A frequency divider 116 is connected to via multiple lines $64_1 \ldots 64_N$ to the control device 42. The number of lines connecting the frequency divider 116 and the control device 42 is equal the number of different dynamic loads that can be connected in turn to the voltage regulator. The frequency divider 116 controls the multiplexer 114, which in turn controls the switched capacitor 112. The operation of switched capacitors such as switched capacitor 112 is described in copending application S.N._____ ,_____ (Attorney's Docket No. 95-L-119) filed September 29, 1995, incorporated herein by reference, said application assigned to SGS-THOMSON Microelectronics, Inc..

At t_2 and t_5 the control device 42 signals to the regulating means to change the bandwidth of the voltage regulator by changing the logic state on the line corresponding to the connected dynamic load 44. The frequency divider 116 supplies the multiplexer 114 with the frequency which will produce a bandwidth at which the transient response time would be shortest for the particular dynamic load 44, this will typically be a high frequency in order to produce a high bandwidth. The multiplexer 114 then sets the effective resistance of the switched capacitor 112 to this frequency. This changes the bandwidth of the voltage regulator 40 to the second bandwidth, thereby reducing the time it takes voltage regulator 40 to begin to deliver the required voltage, i. e., reducing the transient response time.

At t_4 and t_8, when the voltage regulator 40 is delivering required voltage, the control device 42 can again signal to the regulating means to change the bandwidth of the voltage regulator by changing the logic state on the line corresponding to the connected dynamic load 44. The frequency divider 116 supplies the multiplexer 114 with the frequency which will produce the optimal bandwidth for the particular dynamic load 44. The multiplexer 114 then sets the effective resistance of the switched capacitor 112 to this frequency, thereby changing the bandwidth of the voltage regulator 40 to either the first of third bandwidth.

Therefore the invention allows a quick response to the large increase or decrease in current required by the microprocessor 44 of a voltage regulator 40 when the microprocessor 44 is changing its level of power consumption. This is accomplished without compromising the stability of the voltage regulator 40. This is particularly advantageous for systems where a component can enter a power-down mode to reduce its power consumption, such as: battery operated systems where the reduction of power consumption will lead to an increase in battery life, "green" PCs designed to consume less power in an effort to allow more people access to computers without requiring an increase in generated power, and in an effort to preserve natural resources.

While the invention has been specifically described with reference to a preferred embodiment, it will be understood by those of ordinary skill in the prior art having reference to the current specification and drawings that various modifications may be made and various alternatives are possible therein without departing from the spirit and scope of the invention.

For example:

Although the control means is described as being a located outside of the microprocessor, it can be located inside the microprocessor but would remain active when the microprocessor is in the power-down mode.

Additionally, the control device can be any of the various microprocessor auxiliary chips, e.g. chips which include voltage or power-monitoring functions.

While the dynamic load is described as a microprocessor, any other component that can operate in at least two power consumption levels may be used.

Although only one power-down mode is described, the load can operate at several power-down modes.

While the voltage source is described as a battery, any power source may be used.

Additionally while the system is described using a linear voltage regulator a switched regulator may be used without departing form the scope of the invention.

Furthermore, while the invention is described with relation to a computer, the invention can be used in a the electrical system of an automobile, or any other system where a it is advantageous to place at least one of the system's component into a power-down mode to reduce the amount of power consumed by the system, without departing from the scope of the invention.

Claims

1. An electronic system comprising:

   at least one component capable of operating at either of at least two power consumption levels, having a power supply input;
   a power supply including:

   a voltage regulator comprising:

   a first input coupled to a power source;
   a second input; and,
   an output coupled to said power supply input of said component; and

   wherein said voltage regulator regulates current from said power source to provide a voltage at said output which is regulated with a bandwidth which varies in dependence on signals received at said second input.

2. The electronic system according to claim 1, wherein said power source further comprises a battery.

3. The electronic system according to claim 1, further comprising a sensing means for sensing if one of said components is about to be accessed, said sensing means having a first output coupled to a second input of said component, and a second output coupled to said second input of said voltage regulator.

4. The electronic system according to claim 3, further comprising a first notifying means for notifying component to power-up, wherein said first notifying means having an input coupled to said first input of said sensing means and an output coupled to said second input of said component.

5. The electronic system according to claim 3, further comprising a second notifying means for notifying said regulating means to change the bandwidth of said voltage regulator, wherein said second notifying means having an input coupled to said second input of said sensing means and an output coupled said second input of said voltage regulator.

6. The electronic system according to claim 1, wherein said component comprises a microprocessor.

7. A voltage regulator comprising:

a first input node;
an output node;
a second input for regulating the bandwidth of said voltage regulator; and
a regulating means coupled to said second input for changing the bandwidth of said voltage regulator in response to an externally received signal.

8. The voltage regulator according to claim 7, further comprising a dynamic load capable of operating at either of at least two power consumption levels, coupled to said output node.

9. The voltage regulator according to claim 7, wherein said second input is coupled to a control device.

10. The voltage regulator according to claim 7, wherein said first input is coupled to a voltage source.

11. A computer comprising:

a voltage regulator comprising a first input, a second input regulator, an output. and a regulating means for regulating the bandwidth of said voltage regulator coupled to said second input;
a dynamic load, having a first input coupled to said output, and capable of operating at either of at least two levels of power consumption; and,
a control device connected to sense changes in operating conditions, and having a first control output coupled to said second input of said dynamic load, and a second control output coupled to said second input of said voltage regulator;
wherein said regulating means changes the bandwidth of said voltage regulator when said control device activates said first control output.

12. The computer of claim 11, wherein one of said levels of power consumption is a power-down level.

13. The computer of claim 1, 7 or 11, wherein said one of said levels of power consumption is a power-down level.

14. The computer of claim 1, 7 or 11, wherein said means for regulating the bandwidth of said voltage regulator comprises a first analog switch for bypassing a first compensation capacitor of said voltage regulator when said regulating means is changing the bandwidth of said voltage regulator.

15. The computer according to claim 1, 7 or 11, wherein said means for regulating the bandwidth of said voltage regulator comprises:

a plurality of compensation capacitors, each said capacitor providing an optimum operating bandwidth for said dynamic load operating at a power consumption level higher than its lowest power consumption level; and,
a plurality of analog switches for bypassing each said compensation capacitor of said voltage regulator when said regulating means is changing the bandwidth of said voltage regulator.

16. The computer of claim 8 or claim 11, wherein said dynamic load comprises a microprocessor.

17. A method for regulating the voltage of an electronic system having a voltage regulator and at least one component capable of operating at either of at least two levels of power consumption, having an input coupled to an output node of said voltage regulator, comprising:

sensing that said component is about to be accessed;
changing the bandwidth of said voltage regulator to a second bandwidth;
powering up said component.

18. The method of claim 17, further comprising the step of changing the bandwidth of said voltage regulator

from said second bandwidth back to said first bandwidth.

19. The method of claim 18, further comprising the step of sensing that said regulator is delivering the voltage required by said one component, performed after said step of powering up said component and before said step of changing the bandwidth of said voltage regulator from said second bandwidth back to said first bandwidth.

20. The method of claim 17, further comprising the step of changing the bandwidth of said voltage regulator from said second bandwidth to a third bandwidth.

21. The method of claim 20, further comprising the step of sensing that said regulator is delivering the voltage required by said one component, performed after said step of powering up said component and before said step of changing the bandwidth of said voltage regulator from said second bandwidth back to a third bandwidth.

FIG. 1

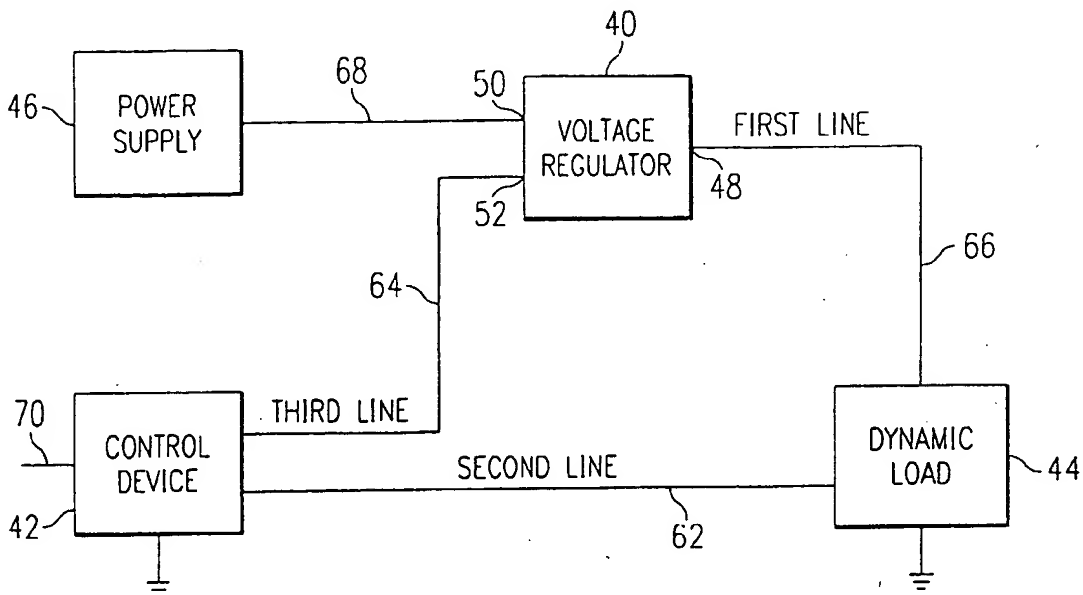
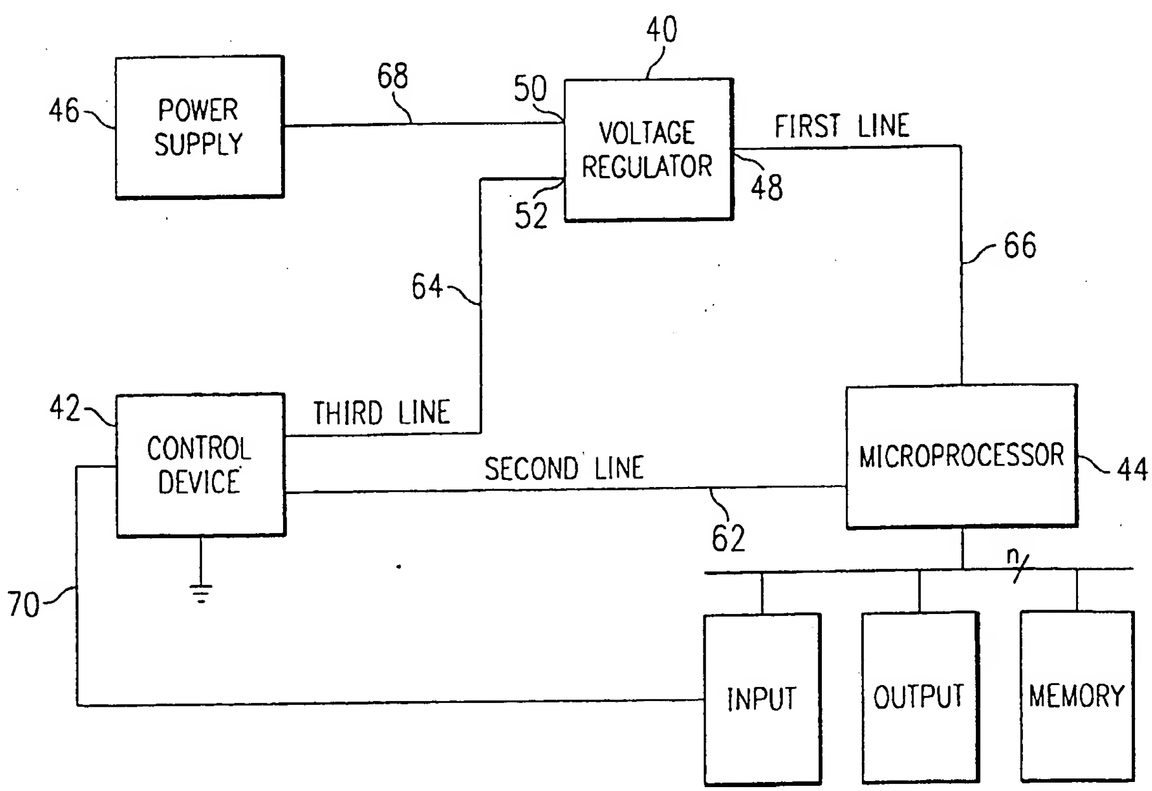

40
68
50
46
POWER SUPPLY
VOLTAGE REGULATOR
FIRST LINE
48
52
66
64
70
CONTROL DEVICE
THIRD LINE
DYNAMIC LOAD
44
SECOND LINE
42
62

FIG. 2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68
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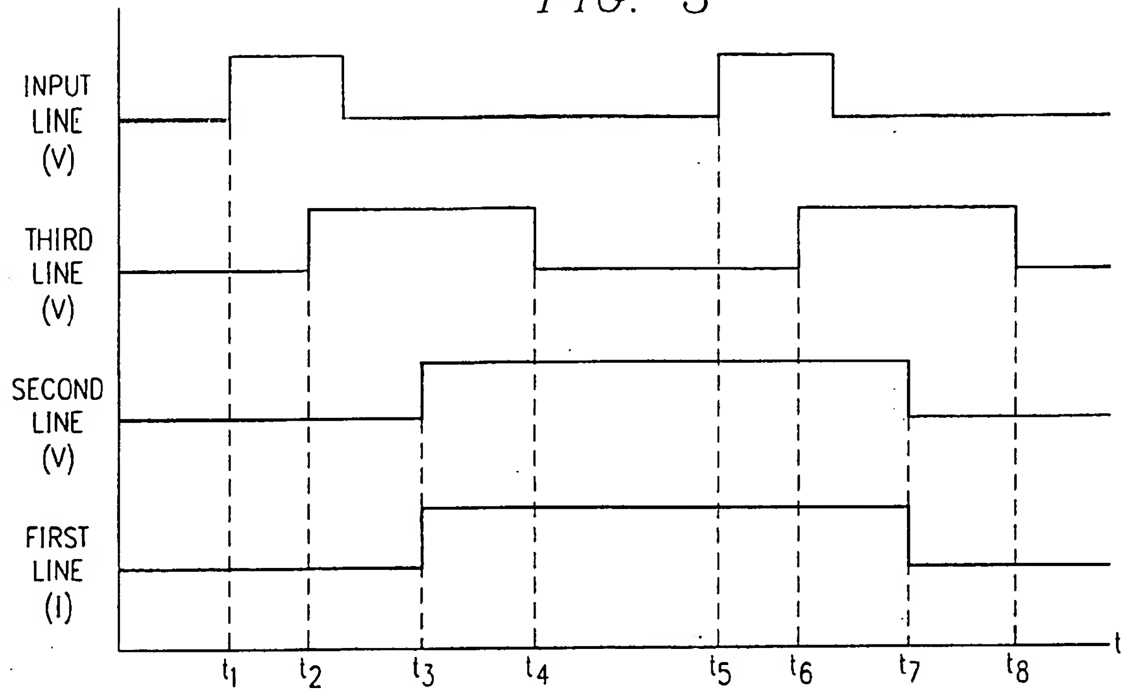
46
POWER SUPPLY
VOLTAGE REGULATOR
FIRST LINE
48
52
66
64
42
CONTROL DEVICE
THIRD LINE
MICROPROCESSOR
44
SECOND LINE
62
n
70
INPUT
OUTPUT
MEMORY

FIG. 3


INPUT LINE (V)
THIRD LINE (V)
SECOND LINE (V)
FIRST LINE (I)
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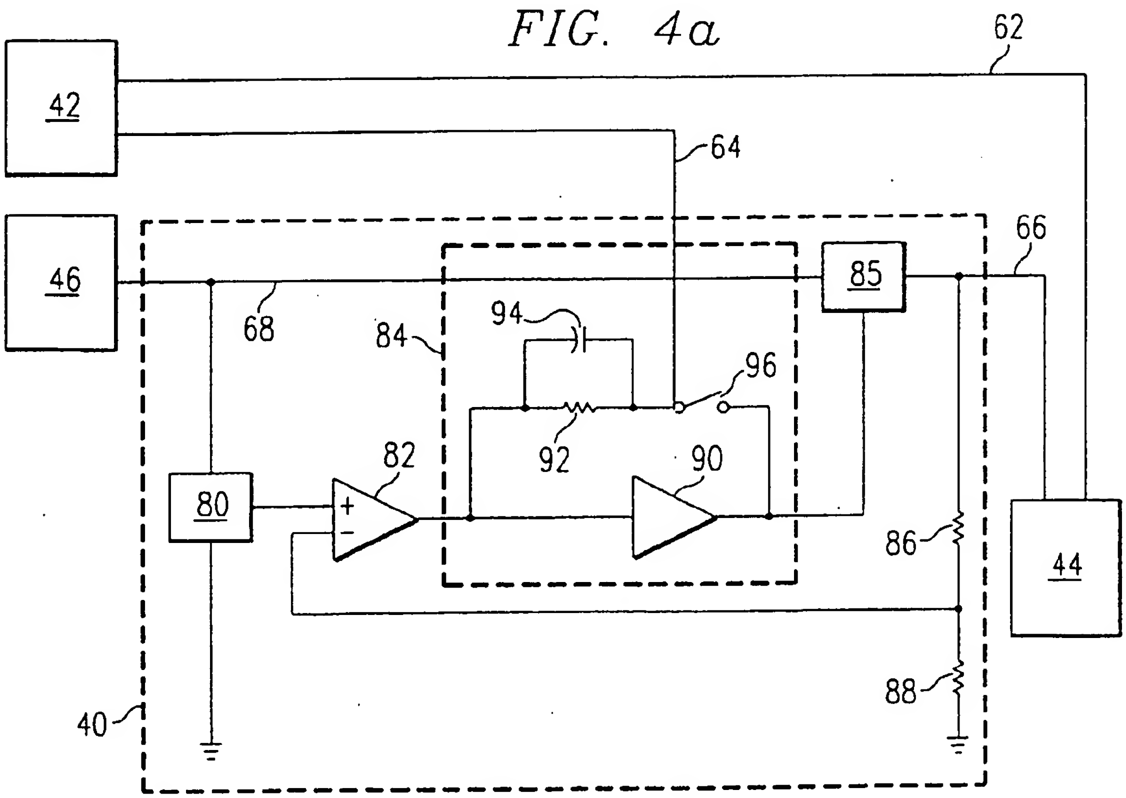
t1
t2
t3
t4
t5
t6
t7
t8

FIG. 4a


62
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64
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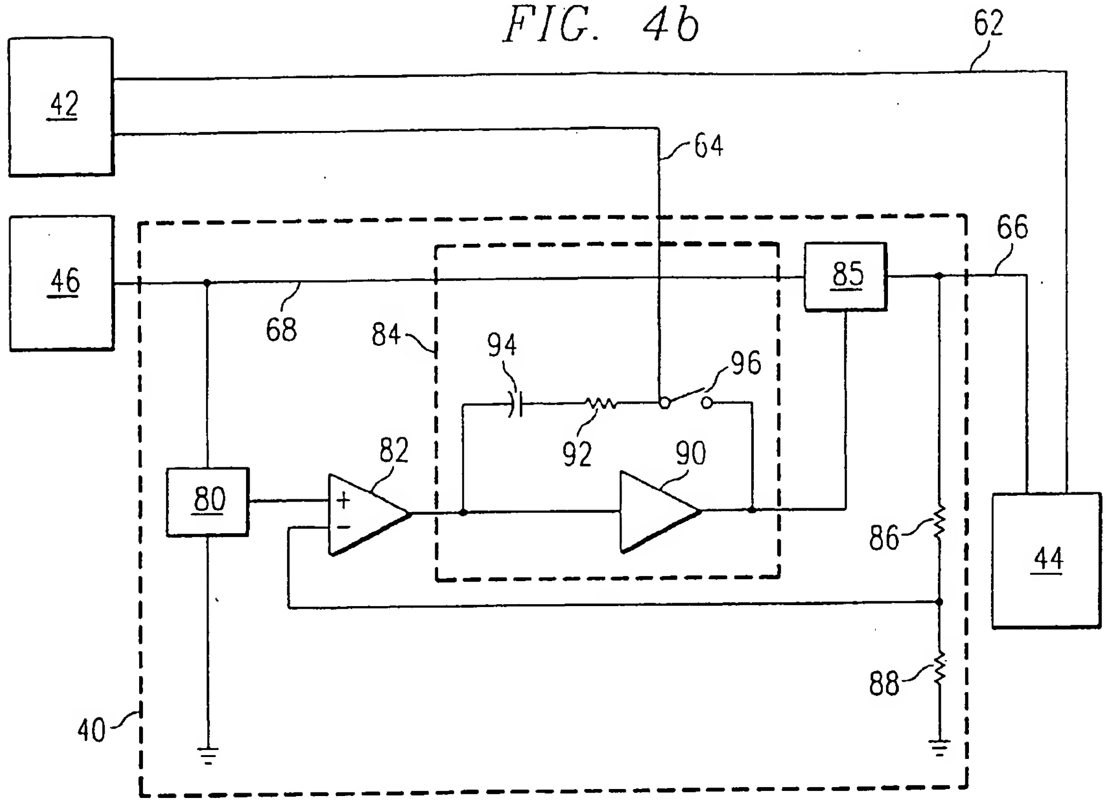
82
80
86
44
88
40

FIG. 4b


62
42
64
46
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85
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84
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90
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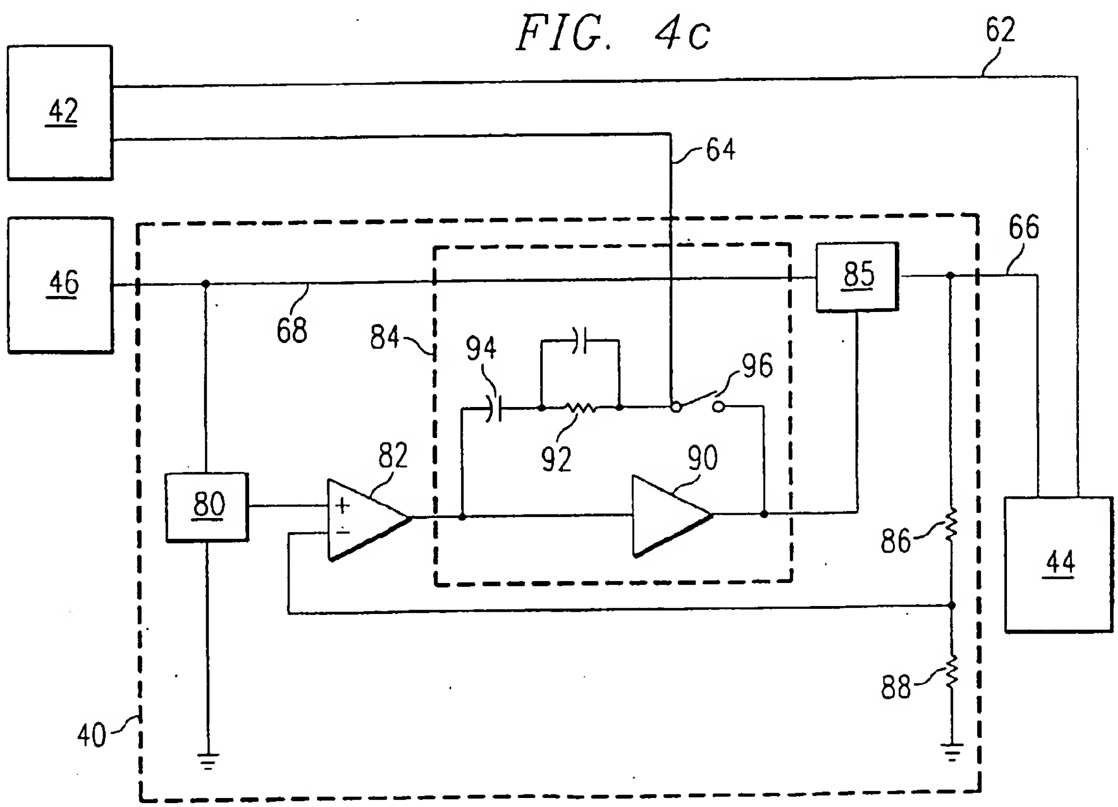
86
44
88
40

FIG. 4c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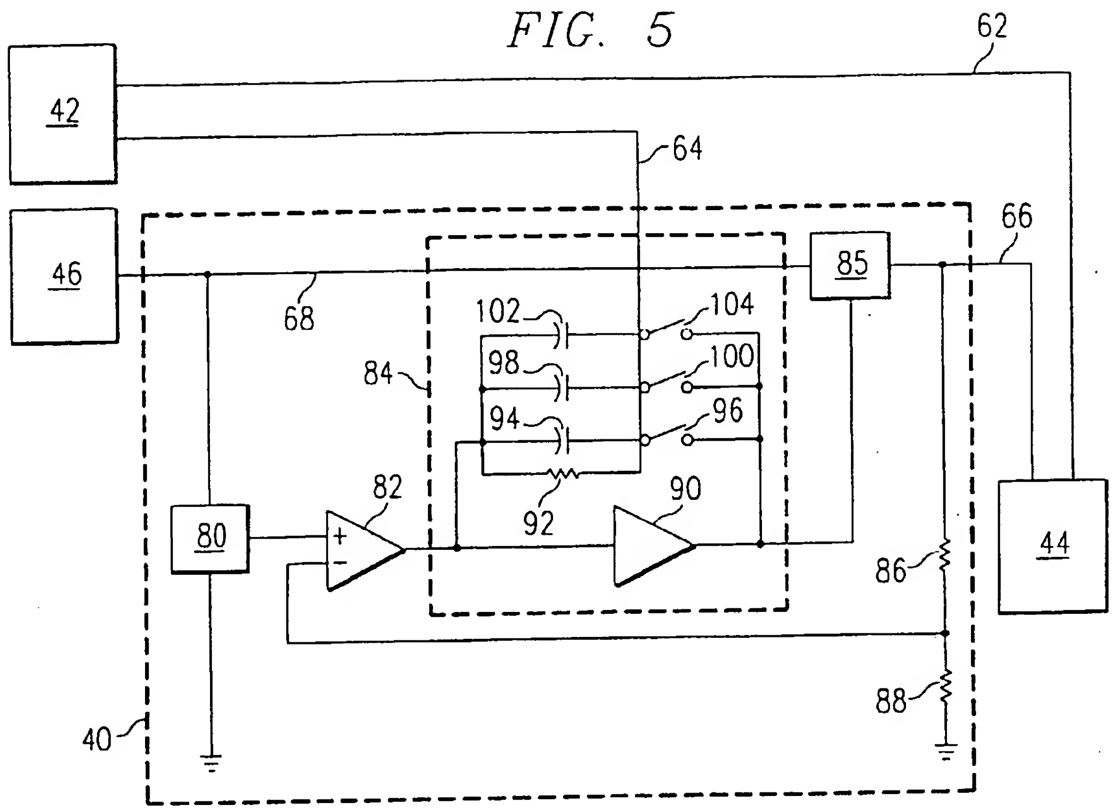
FIG. 5
62
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102
104
98
100
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44

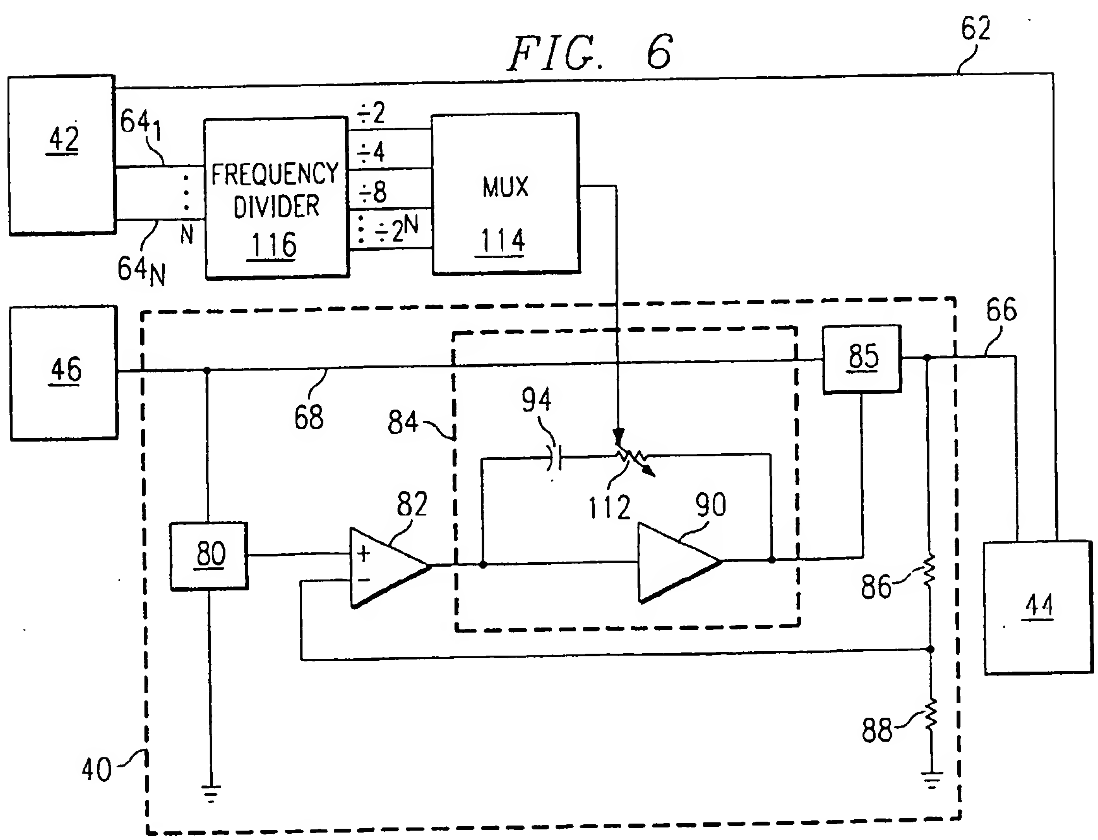
FIG. 6
62
42
64_1
FREQUENCY DIVIDER
116
÷2
÷4
÷8
÷2^N
MUX
114
N
64_N
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85
66
68
84
94
112
90
82
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86
88
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44

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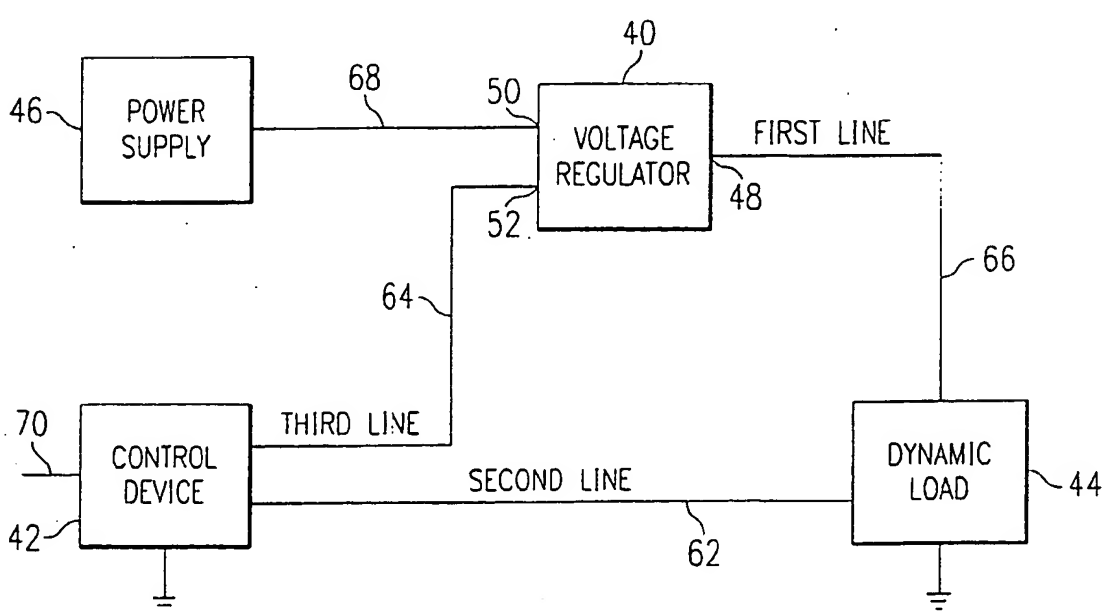
(54) **Programmable bandwidth voltage regulator**

(57) A method for reducing the transient response time of a voltage regulator when the load attached to it is entering or exiting a lower power consumption level by changing the bandwidth of the voltage regulator without compromising its stability, and a bandwidth regulator for implementing such a method are disclosed, wherein the bandwidth of the voltage regulator is changed based on a signal sent by a control device when it senses that the component is about to change power consumption levels.

FIG. 1



0 779 568 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 96 30 8927

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 191 278 A (CARPENTER BRIAN A) 2 March 1993 * the whole document * ---	1,2,9,12	G05F3/26 G05F1/565
A	US 4 908 566 A (TESCH BRUCE J) 13 March 1990 * column 1, line 17 - column 2, line 38 * ---	1,2,9,12	
A	US 5 168 209 A (THIEL V FRANK L) 1 December 1992 * column 1, line 21 - column 3, line 37 * ---	1,2,9,12	
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A	ELECTRONIC DESIGN, vol. 42, no. 17, 22 August 1994, page 123/124, 126, 128 XP000491516 O'MALLEY K: "UNDERSTANDING LINEAR-REGULATOR COMPENSATION" * the whole document * ---	1	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G05F
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 April 1997	Schobert, D

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